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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/711,556	09/24/2004	Patrick J. McGinnis	FIS920040161	FIS920040161 5555	
32074	7590 08/09/2005		EXAMINER		
	ΓΙΟΝΑL BUSINESS ΜΑ	NGUYEN, JIMMY			
DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			ART UNIT	PAPER NUMBER	
			2829		
			DATE MAILED: 08/09/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
Office Action Summary		10/711,556	MCGINNIS ET AL.			
		Examiner	Art Unit			
	·	Jimmy Nguyen	2829			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1)⊠	Responsive to communication(s) filed on 24 M	lay 2005.				
2a)□		action is non-final.				
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
5) 🗌						
Applicat	ion Papers	•				
9) 🗌	The specification is objected to by the Examine	er.				
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
2) Notice 3) Infor	et(s) ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) er No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Di 5) Notice of Informal F 6) Other:				

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DETAILED ACTION

Claims objection

Claims 21 and 29 are objected because the newly limitation " means for disposing DUT within a scanning chamber" is no where to be found in the drawing and specification. Further, is the limitation "means for repeatedly applying said predefined stimulus to semiconductor device" part of ATE or totally different component that perform this function. Clarification is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 2. Claims 21 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Perdu et al. (US 2005/0006602 A1).

As to claims 21, 29 - 31, Perdu et al disclosed (figs 1 - 3) a system and a method for critical parameter analysis (CPA) of a semiconductor device (DUT, 2), comprising:

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A laser scanning microscope (14);

ATE (6) for providing predefined stimulus to the DUT (2) for comparing responses from the DUT against a set of predefined expected responses (column 3 paragraph 27), and for generating a short output pulse when a difference is detected between responses from DUT and predefined expected response;

Means for disposing DUT (2) within a scanning chamber of laser scanning microscope while DUT (2) is connected to ATE (26);

Display (20, column 3 paragraph 35) means for displaying an image of semiconductor device (2) produced by LSM (14);

Means for overlaying a visible representation (column 3 paragraph 27) of short output pulse on displayed image (20) to indicate a corresponding position on the DUT (2) of a scanning beam of the LSM at the time the output pulse was generated; and

means for repeatedly applying predefined stimulus (by ATE 26) to said semiconductor device DUT (2) and comparing response therefrom against said predefined expected response while simultaneously scanning said semiconductor device (2) with laser LSM (14);

wherein the automated test apparatus (A'FE, 26) and the semiconductor device (DUT, 2) form a closed loop feedback system;

wherein the automated lest apparatus (ATE, 26) is programmed to 'break' in or out of a vector loop (column 2 paragraph 24) which is detecting pass/fail operation of the semiconductor device; and

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wherein automated test apparatus (ATE, 26) is configured to repeatedly cycle (short cycle) said predefined stimulus from point up to a point of failure when such failure is detected (column 2 paragraph 24 – column 3 paragraph 24).

As to claims 22, 34, Perdu et al disclosed (figs 1 - 3) a system and a method wherein semiconductor device (DUT, 2) is fixtured such that ATE (26) connections to the device are made within a scanning chamber of the focused optical beam scanning device (14).

As to claims 23, 35, Perdu et al disclosed (figs 1 - 3) a system and a method further comprising:

Image converting means for representing output from the laser scanning microscope (14) as a viewable video signal (column 3 paragraph 35) and for overlaying the output signal (column 3 paragraph 27) indication from the ATE (26) on viewable video signal; and

Display (20) means for viewing video signal with overlaid ATE output signal indication.

As to claims 24, 36, Perdu et al disclosed (figs 1 - 3) a system and a method wherein overlaid ATE (26) output signal indication produces a visible spot on display (20) means at a location on a simultaneously displayed image (column 2 paragraph 24 – column 3 paragraph 24) of the DUT (2) that indicates the location on the DUT (2) that

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was illuminated by the laser (14) at the time ATE output signal indication was produced.

As to claims 25, 37, Perdu et al disclosed (figs 1 - 3) a system wherein predefined stimulus is provided to ATE in the form of a set of test vectors (column 2 paragraph 24).

As to claims 26, 38, Perdu et al disclosed (figs 1 - 3) a system wherein predefined expected responses are provided to ATE in the form of a set of test vectors (column 2 paragraph 24).

As to claims 27, 39, Perdu et al disclosed (figs 1 - 3) a system wherein ATE (26) is configured to repeatedly apply predefined stimulus to DUT (2) in a test loop.

As to claims 28, 40, Perdu et al disclosed (figs 1 - 3) a system wherein output pulse is a short pulse generated when a difference is detected between responses by DUT (2) to predefined stimulus and the predefined expected responses.

As to claim 32, Perdu et al disclosed (figs 1 - 3) a method further comprising providing optical signatures that only appear on the gate level devices responsible for the failing test.

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As to claim 33, Perdu et al disclosed (figs 1 - 3) a method further comprising providing real time feedback to the focused optical beam scanning device (140 and subsequent optical images acquired.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is (703) 306-5858. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramiz Nestor, can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jimmy Nguyen

8/5/2005

VINH NGUYEN PRIMARY EXAMINER

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